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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,869	04/07/2006	Walter Fix	411000-144	6418

27162 7590 12/16/2008

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EXAMINER	
MONTALVO, EVA Y	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
12/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,869	FIX ET AL.	
	Examiner	Art Unit	
	Eva Montalvo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3, and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/02/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action responds to the amendment filed on 08/12/2008.

Acknowledgement

2. The amendment filed on 08/12/2008, responding to the Office action mailed on 05/14/2008, has been entered into the record. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this office action are claims 1, 3 and 8.

Specification

3. Claim 3 is objected to because of the following informalities:

Claim 3, line 3, "overlapping the one source/drain electrode" should read --overlapping one source/drain electrode--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (US 2002/0047839 and Kasai hereinafter) in view of Mutsaers et al. (US 6,429,450 and Mutsaers hereinafter).

Kasai discloses a logic gate comprising a circuit (see fig. 4) having an output and comprising at least one charging field effect transistor (charging FET) (i.e., Tr1) on a substrate, and at least one switching field effect transistor (switching FET) (i.e., Tr4) having at least one gate electrode, a source electrode and a drain electrode, the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source and a reference potential such that the gate electrode of the charging FET is not connected via an electrical line directly to the voltage source, to the reference potential, to the input, or to the output, wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET.

Although the device disclosed by Kasai shows substantial features of the claimed invention, it fails to expressly teach that the FET is organic and the charging FET including a first structured layer comprising source and drain followed by a semiconductor layer on the electrodes followed by a layer of insulating material on the semiconductor layer and adjacent to and contiguous with a second electrode layer.

Nonetheless, these features are well known in the art and would have been an obvious modification of the device disclosed by Kasai, as evidenced by Mutsaers.

Mutsaers discloses a device comprising an organic FET (see Fig. 2) and the FET including a first structured layer (3) comprising source and drain (32 and 33) followed by a semiconductor layer (4) on the electrodes followed by a layer of insulating material (5) on the semiconductor layer and adjacent to and contiguous with a second electrode layer (6).

Given the teachings of Mutsaers, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Kasai, as suggested by Mutsaers, by employing an organic FETs in the circuit. This would provide a simple and cost effect way of manufacture FETs utilized in the integrated circuits when comparing to silicon technologies (see col. 1, lines 14-28 and col. 2, lines 29-55).

7. As to claims 3 and 8, Mutsaers discloses a device, where the gate electrode of the charging FET overlapping one source/drain electrode of the charging FET (see Fig. 2); and the organic logic gate is constructed without plated-through holes (see Fig. 1 and 2). The examiner notes that Mutsaers does not disclose a logic gate constructed with plated-through holes.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 3 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Montalvo whose telephone number is (571)270-3829. The examiner can normally be reached on Monday through Thursday 7:30-5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marcos D. Pizarro-Crespo can be reached on (571)272-1716. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eva Montalvo
Patent Examiner
Art Unit 2814

/Marcos D. Pizarro/
Primary Examiner, Art Unit 2814